REMARKS

The Office Action dated April 21, 2006, has been received and reviewed.

Claims 1-13, 17-26, 31-33, 37-39, and 42-44 are currently pending and under consideration in the above-referenced application. Each of claims 1-13, 17-26, 31-33, 37-39, and 42-44 stands rejected.

Claims 14-16, 27-30, 34-36, 41, and 45-67 are withdrawn from consideration. Claims 40 and 68-102 have been canceled without prejudice or disclaimer.

Reconsideration of the above-referenced application is respectfully requested.

Rejections under 35 U.S.C. § 103(a)

Claims 1-13, 17-26, 31-33, 37-39, and 42-44 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Nakanishi

Claims 1-10, 17, 19-26, 33, 37-39, and 42-44 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent Publication 2001/0013643 of Nakanishi et al. (hereinafter "Nakanishi").

Independent claim 1 is directed to a semiconductor device that includes a semiconductor die and a dielectric spacer layer formed on and secured to at least a portion of a surface of the semiconductor die. The dielectric spacer layer of independent claim 1 includes "voids communicating with a lateral periphery thereof."

It is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1 because Nakanishi does not teach or suggest a semiconductor device that includes a dielectric spacer layer with a void that "communicat[es] with a lateral periphery" of the dielectric spacer layer. Rather, the teachings of Nakanishi are limited to a polyimide spacer 24 (paragraph **[0078]**) that is "disposed along the periphery of the region where the semiconductor chips **1** and **2** are stacked" to provide for "a high level of accuracy in the balance of the intervals between the semiconductor chips **1** and **2**" (paragraph **[0080]**). While FIG. 9 of Nakanishi shows the polyimide spacer 24 as being positioned adjacent to opposite peripheral edges of the stacked assembly and, thus, including a central void, it should be noted that FIG. 9 is a cross section. Thus, the entire extent of the polyimide spacer 24 is not shown. Nor does FIG. 9 show (*i.e.,* teach or suggest) that the central void may communicate with a lateral periphery of the polyimide tape 24.

As Nakanishi does not teach or suggest each and every element of independent claim 1, it is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1. As such, the subject matter to which independent claim 1 is directed is, under 35 U.S.C. § 103(a), allowable over the subject matter taught in Nakanishi.

Each of claims 2-10 and 17 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 2 is further allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof may include a plurality of laterally discrete spacers.

Claim 5 is also allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof may have a thickness that exceeds a height that at least one intermediate conductive element (*e.g.,* bond wires 8a, 8b of FIG. 9) protrudes above the active surface of a semiconductor device 2, 3 to which the polyimide spacer is secured.

Claim 8 is additionally allowable because Nakanishi teach or suggest that the polyimide spacer 24 thereof comprises a pattern.

Claim 9 is further allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof comprises randomly arranged features.

Claim 17 is also allowable because Nakanishi does not teach or suggest that adhesive material may be present on an exposed surface of the polyimide spacer 24.

Independent claim 19 is drawn to a semiconductor device assembly that includes, among other things, a nonconfluent spacer layer that spaces an active surface of a first semiconductor device apart from a back side of a second semiconductor device.

In contrast to the subject matter recited in independent claim 19, the teachings of Nakanishi are limited to assemblies with spacer layers that separate active surfaces of semiconductor devices apart from one another. *See, e.g.,* Fig. 9; paragraphs **[0077]** and **[0047]**. As Nakanishi does not teach or suggest an assembly in which a spacer layer spaces an active surface of a first semiconductor device apart from a back side of a second semiconductor device, Nakanishi cannot be relied upon to establish a *prima facie* case of obviousness against independent claim 19.

Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 19 is allowable over the subject matter taught in Nakanishi.

Claims 20-26, 33, 37-39, and 42-44 are each allowable, among other reasons, for depending directly or indirectly from claim 19, which is allowable.

Claim 20 is also allowable since Nakanishi neither teaches nor suggests that the polyimide spacer 24 thereof includes at least one void that communicates with a lateral periphery of the polyimide spacer 24.

Claim 21, which depends from claim 20, is additionally allowable because Nakanishi does not teach or suggest that the polyimide spacer 24 includes a void that facilitates introduction of adhesive material between first and second semiconductor devices.

Claim 22 is further allowable since Nakanishi includes no teaching or suggestion that the polyimide spacer 24 thereof includes a plurality of laterally discrete spacers.

Claim 24 is additionally allowable because Nakanishi does not teach or suggest an assembly in which an intermediate conductive element is located at least partially between first and second semiconductor devices that are spaced apart from one another by the polyimide spacer 24 disclosed therein.

Claim 25 depends from claim 24 and is also allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof may space first and second semiconductor devices apart from one another a distance that exceeds a height that at least one intermediate conductive element (*e.g.*, bond wires 8a, 8b of FIG. 9) protrudes above the active surface of one of the semiconductor devices 2, 3.

Claim 33 is additionally allowable because Nakanishi teach or suggest that the polyimide spacer 24 thereof comprises a pattern.

Nakanishi in View of Smith

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Nakanishi, in view of teachings from U.S. Patent 6,049,370 to Smith, Jr. et al. (hereinafter "Smith").

Claims 11 and 12 are allowable, among other reasons, for depending from claim 1, which is allowable.

Nakanishi in View of Blanton

Claims 18 and 31 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over the subject matter taught in Nakanishi, in view of teachings from U.S. Patent 5,220,200 to Blanton (hereinafter "Blanton").

Claim 18 is allowable, among other reasons, for depending from claim 1, which is allowable.

Claim 31 is allowable, among other reasons, for depending from claim 19, which is allowable.

Nakanishi in View of Mueller

Claims 11, 13, and 32 stand rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly not patentable over the subject matter taught in Nakanishi, in view of the teachings of U.S. Patent 6,316,786 to Mueller et al. (hereinafter "Mueller").

Claims 11 and 13 are both allowable, among other reasons, for depending directly from claim 1, which is allowable.

Claim 32 is allowable, among other reasons, for depending directly from claim 19, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-13, 17-26, 31-33, 37-39, and 42-44 be withdrawn.

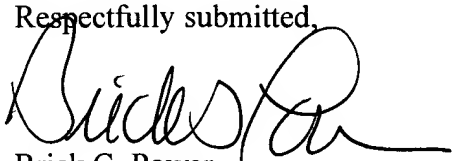
ELECTION OF SPECIES REQUIREMENT

Independent claim 1 remains generic to all of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41, and 45-67, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

CONCLUSION

It is respectfully submitted that each of claims 1-39 and 41-67 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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